L Number	Hits	Search Text	DB	Time stamp
1	2	power with cache with ((microinstruction or micro-instruction) or uop)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:05
2	422	((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:06
3	244	((power adj control) or (power$3 adj down) or (conserv$3 adj power)) with cache	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:07
4	7	(((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and (((power adj control) or (power$3 adj down) or (conserv$3 adj power)) with cache)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:07
5	1331	tag adj write or tag adj read or tag adj inquiry	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:08
6	36	(((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and (tag adj write or tag adj read or tag adj inquiry)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:08
7	11193401	@ad<20001228	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:09
8	35	((((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and (tag adj write or tag adj read or tag adj inquiry)) and @ad<20001228	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:09
9	10509	(microinstruction or micro-instruction) or uop	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:13
10	33	(((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and ((microinstruction or micro-instruction) or uop)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:13
11	31	@ad<20001228 and ((((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and ((microinstruction or micro-instruction) or uop))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:13
12	3056	way with (disable or disabled)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:14
13	2	((((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and ((microinstruction or micro-instruction) or uop)) and (way with (disable or disabled))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:14
14	0	(@ad<20001228 and ((((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and ((microinstruction or micro-instruction) or uop))) and (way with (disable or disabled))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:14
15	28	(tag adj write or tag adj read or tag adj inquiry) and (way with (disable or disabled))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:15
16	4	(((disabl$3 or turn-off or turn adj off or shut adj down) with cache) same instruction) and ((tag adj write or tag adj read or tag adj inquiry) and (way with (disable or disabled)))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:15

17	1449	711/154.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:15
18	445	711/128.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:15
19	360	711/136.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:15
20	666	711/133.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:15
21	604	711/156.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:15
22	678	713/320.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:16
23	498	713/322.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:16
24	485	713/324.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/04/25 15:16

Inventor Name Search Result

Your Search was:

Last Name = MAIYURAN
First Name = SUBRAMANIAM

Application#	Patent#	Status	Date Filed	Title	Inventor Name 33
10739689	Not Issued	020	12/17/2003	METHOD AND APPARATUS FOR A STEW-BASED LOOP PREDICTOR	MAIYURAN, SUBRAMANIAM
10732505	Not Issued	020	12/09/2003	DYNAMICALLY CONFIGURABLE CLOCKING SCHEME FOR DEMAND BASED RESOURCE SHARING WITH MULTIPLE CLOCK CROSSING DOMAINS	MAIYURAN, SUBRAMANIAM
10654573	Not Issued	030	09/02/2003	MFENCE AND LFENCE MICRO-ARCHITECTURAL IMPLEMENTATION METHOD AND SYSTEM	MAIYURAN, SUBRAMANIAM
10646033	Not Issued	030	08/22/2003	METHOD AND APPARATUS FOR A TRACE CACHE TRACE-END PREDICTOR	MAIYURAN, SUBRAMANIAM
10607979	Not Issued	030	06/30/2003	LOOK AHEAD LRU ARRAY UPDATE SCHEME TO MINIMIZE CLOBBER IN SEQUENTIALLY ACCESSED MEMORY	MAIYURAN, SUBRAMANIAM
10318510	Not Issued	030	12/13/2002	THROTTLE OF AN INTEGRATED DEVICE	MAIYURAN, SUBRAMANIAM
10206748	Not Issued	093	07/26/2002	METHOD AND APPARATUS FOR CACHE REPLACEMENT FOR A MULTIPLE VARIABLE-WAY ASSOCIATIVE CACHE	MAIYURAN, SUBRAMANIAM
10194531	6651151	150	07/12/2002	MFENCE AND LFENCE MICRO-ARCHITECTURAL IMPLEMENTATION METHOD AND SYSTEM	MAIYURAN, SUBRAMANIAM
10170171	Not Issued	041	06/11/2002	APPARATUS, METHOD, AND SYSTEM FOR SYNCHRONIZING INFORMATION PREFETCH BETWEEN PROCESSORS AND MEMORY CONTROLLERS	MAIYURAN, SUBRAMANIAM
10051008	Not Issued	071	01/22/2002	METHOD AND APPARATUS TO HANDLE MULTIPLE REQUESTS TO DIFFERENT MEMORY AGENTS	MAIYURAN, SUBRAMANIAM
09966587	6718440	150	09/28/2001	MEMORY ACCESS LATENCY HIDING WITH HINT BUFFER	MAIYURAN, SUBRAMANIAM
09962716	6507219	150	09/21/2001	CHARGE SHARING AND CHARGE RECYCLING FOR AN ON-CHIP BUS	MAIYURAN, SUBRAMANIAM
09758486	6526499	150	01/10/2001	METHOD AND APPARATUS FOR LOAD BUFFERS	MAIYURAN, SUBRAMANIAM
09750750	Not Issued	071	12/27/2000	SYSTEM AND METHOD FOR CACHE SHARING	MAIYURAN, SUBRAMANIAM
09749750	Not Issued	071	12/28/2000	LOW POWER CACHE ARCHITECTURE	MAIYURAN, SUBRAMANIAM J.
09723288	Not Issued	061	11/28/2000	CACHE DYNAMICALLY CONFIGURED FOR SIMULTANEOUS ACCESSES BY MULTIPLE COMPUTING ENGINES	MAIYURAN, SUBRAMANIAM
09675096	Not	041	09/28/2000	METHOD AND APPARATUS FOR THE	MAIYURAN, SUBRAMANIAM

	Issued			IMPLEMENTATION OF FULL-SCENE ANTI-ALIASING SUPERSAMPLING	
09667688	6665775	150	09/22/2000	CACHE DYNAMICALLY CONFIGURED FOR SIMULTANEOUS ACCESSES BY MULTIPLE COMPUTING ENGINES	MAIYURAN, SUBRAMANIAM
09665923	Not Issued	061	09/20/2000	OPPORTUNISTIC SHARING OF GRAPHICS RESOURCES TO ENHANCE CPU PERFORMANCE IN AN INTEGRATED MICROPROCESSOR	MAIYURAN, SUBRAMANIAM
09657559	6735712	150	09/08/2000	DYNAMICALLY CONFIGURABLE CLOCKING SCHEME FOR DEMAND BASED RESOURCE SHARING WITH MULTIPLE CLOCK CROSSING DOMAINS	MAIYURAN, SUBRAMANIAM
09609072	6438658	150	06/30/2000	FAST INVALIDATION SCHEME FOR CACHES	MAIYURAN, SUBRAMANIAM
09608507	Not Issued	041	06/30/2000	METHOD AND APPARATUS FOR CACHE REPLACEMENT FOR A MULTIPLE VARIABLE-WAY ASSOCIATIVE CACHE	MAIYURAN, SUBRAMANIAM
09606837	6604162	150	06/28/2000	SNOOP STALL REDUCTION ON A MICROPROCESSOR EXTERNAL BUS	MAIYURAN, SUBRAMANIAM
09475759	6546462	150	12/30/1999	CLFLUSH MICRO-ARCHITECTURAL IMPLEMENTATION METHOD AND SYSTEM	MAIYURAN, SUBRAMANIAM
09475363	6678810	150	12/30/1999	MFENCE AND LFENCE MICRO-ARCHITECTURAL IMPLEMENTATION METHOD AND SYSTEM	MAIYURAN , SUBRAMANIAM
09368639	6356115	150	08/04/1999	CHARGE SHARING AND CHARGE RECYCLING FOR AN ON-CHIP BUS	MAIYURAN , SUBRAMANIAM
09053932	6216215	150	04/02/1998	METHOD AND APPARATUS FOR SENIOR LOADS	MAIYURAN , SUBRAMANIAM
09053387	6205520	150	03/31/1998	METHOD AND APPARATUS FOR IMPLEMENTING NON-TEMPORAL STORES	MAIYURAN , SUBRAMANIAM
09053384	6122715	150	03/31/1998	METHOD AND SYSTEM FOR OPTIMIZING WRITE COMBINING PERFORMANCE IN A SHARED BUFFER STRUCTURE	MAIYURAN , SUBRAMANIAM
09053383	6643745	150	03/31/1998	METHOD AND APPARATUS FOR PREFETCHING DATA INTO CACHE	MAIYURAN , SUBRAMANIAM
09053377	6073210	150	03/31/1998	SYNCHRONIZATION OF WEAKLY ORDERED WRITE COMBINING OPERATIONS USING A FENCING MECHANISM	MAIYURAN , SUBRAMANIAM
09053231	6356270	150	03/31/1998	EFFICIENT UTILIZATION OF WRITE-COMBINING BUFFERS	MAIYURAN , SUBRAMANIAM
09052883	6175253	150	03/31/1998	FAST BI-DIRECTIONAL TRISTATEABLE LINE DRIVER	MAIYURAN, SUBRAMANIAM

Inventor Search Completed: No Records to Display.

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Last Name = MOULTON
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Application#	Patent#	Status	Date Filed	Title	Inventor Name 4
09749750	Not Issued	071	12/28/2000	LOW POWER CACHE ARCHITECTURE	MOULTON, LYMAN
08440035	5644744	150	05/12/1995	A SUPERSCALER INSTRUCTION PIPELINE HAVING BOUNDARY IDENTIFICATION LOGIC FOR VARIABLE LENGTH INSTRUCTIONS	MOULTON, , LYMAN H.
08440034	5625787	150	05/12/1995	A SUPERSCALER INSTRUCTION PIPELINE USING ALIGNMENT LOGIC RESPONSIVE TO BOUNDARY IDENTIFICATION LOGIC FOR ALIGNING AND APPENDING VARIABLE LENGTH INSTRUCTIONS TO INSTRUCTIONS STORED IN CACHE	MOULTON , LYMAN H.
08360520	5640526	150	12/21/1994	A SUPERSCALER INSTRUCTION PIPELINE HAVING BOUNDARY IDENTIFICATION LOGIC FOR VARIABLE LENGTH INSTRUCTIONS	MOULTON , LYMAN H.

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